IN THE CLAIMS

1. (currently amended) A method of identifying one or more defective shift register latches in a scan chain, the method comprising:

electrically coupling a plurality of shift register latches into a series configuration so as to form a scan chain circuit, wherein each of the shift register latches includes a first latch and a second latch connected in a master-slave configuration, wherein each of the first latch and second latch includes at least one clock input;

placing the scan chain circuit into an operating region;

loading a scan test pattern into the scan chain circuit;

placing the scan chain circuit into a failing region;

applying a shift clock pulse to the clock input of the second latch, wherein the shift clock pulse is applied while the scan chain circuit is in the failing region;

placing the scan chain circuit into an operating region; ~~and~~

unloading the scan chain circuit.; and

identifying at least one defective shift register latch in the scan chain circuit.

2. (currently amended) The method of claim 1, further comprising:

analyzing output from the scan chain circuit~~results~~ after the unloading ~~step~~.

3. (original) The method of claim 1, wherein the loading a scan test pattern into the scan chain circuit includes loading a scan test pattern of all zeroes.

4. (currently amended) The method of claim 1, wherein the loading a scan test pattern into the scan chain circuit includes loading of all ones.[[.]]

5. (original) The method of claim 1, wherein the loading a scan test pattern into the scan chain circuit includes loading zero and ones.

6. (original) The method of claim 5, wherein the loading a scan test pattern into the scan chain circuit includes loading an algorithmic scan test pattern.

7. (currently amended) The method of claim 1, wherein the unloading ~~step~~ comprises:

applying a scan clock pulse to the clock input of the first latch and a shift clock pulse to the input of the second latch, wherein the scan pulse and the shift clock pulse are applied while the scan chain circuit is in the operating region;

measuring an output of the second latch against an expected response;

recording the ~~result~~output;

checking whether the scan chain circuit has been completed; and

repeating the applying the scan clock pulse and the shift clock pulse, the measuring the output of the second latch, and the recording ~~steps~~ until the scan chain circuit is completed.

8. (currently amended) A method of identifying one or more defective shift register latches in a scan chain, the method comprising:

electrically coupling a plurality of shift register latches into a series configuration so as to form a scan chain circuit, wherein each of the shift register latches includes a first latch and a second latch connected in a master-slave configuration, wherein each of the first latch and second latch includes at least one clock input;

placing the scan chain circuit into an operating region;

loading a scan test pattern into the scan chain circuit;

placing the scan chain circuit into a failing region;

applying a scan clock pulse to the clock input of the first latch, wherein the scan clock pulse is applied while the scan chain circuit is in the failing region;

placing the scan chain circuit into an operating region;

applying a shift clock pulse to the clock input of the second latch, wherein the shift clock pulse is applied while the scan chain circuit is in the operating region; ~~and~~

unloading the scan chain circuit.; and

identifying at least one defective shift register latch in the scan chain circuit.

9. (currently amended) The method of claim 8, further comprising:
analyzing output from the scan chain circuit~~results~~ after the unloading ~~step~~ the scan chain.

10. (original) The method of claim 8, wherein the loading a scan test pattern into the scan chain circuit includes loading a scan test pattern of all zeroes.

11. (original) The method of claim 8, wherein the loading a scan test pattern into the scan chain circuit includes loading a scan test pattern of all ones.

12. (original) The method of claim 8, wherein the loading a scan test pattern into the scan chain circuit includes loading zero and ones.

13. (original) The method of claim 12, wherein the loading a scan test pattern into the scan chain circuit includes loading an algorithmic scan test pattern.

14. (currently amended) The method of claim 8, wherein the unloading ~~step~~ comprises:

applying a scan clock pulse to the clock input of the first latch and a shift clock pulse to the input of the second latch, wherein the scan pulse and the shift clock pulse are applied while the scan chain circuit is in the operating region;

measuring an output of the second latch against an expected response;

recording the ~~result~~output;

checking whether the scan chain circuit has been completed; and

repeating the applying the scan clock pulse and the shift clock pulse, the measuring the output of the second latch, and the recording ~~steps~~ until the scan chain circuit is completed.

15. (currently amended) A method of identifying one or more defective shift register latches in a scan chain, the method comprising:

electrically coupling a plurality of shift register latches into a series configuration so as to form a scan chain circuit, wherein each of the shift register latches includes a

first latch and a second latch connected in a master-slave configuration, wherein each of the first latch and second latch includes at least one clock input;

placing the scan chain circuit into an operating region;

loading a scan test pattern into the scan chain circuit;

placing the scan chain circuit into a failing region;

applying a scan clock pulse to the clock input of the first latch, wherein the scan clock pulse is applied while the scan chain circuit is in the failing region;

applying a shift clock pulse to the clock input of the second latch, wherein the shift clock pulse is applied while the scan chain circuit is in the failing region;

placing the scan chain circuit into an operating region; ~~and~~

unloading the scan circuit.; and

identifying at least one defective shift register latch in the scan chain circuit.

16. (original) The method of claim 15, further comprising:

applying a shift clock pulse to the clock input of the second latch prior to unloading the latch.

17. (original) The method of claim 15, wherein the loading a scan test pattern into the scan chain circuit includes loading a scan test pattern of all zeroes.

18. (original) The method of claim 15, wherein the loading a scan test pattern into the scan chain circuit includes loading a scan test pattern of all ones.

19. (original) The method of claim 15, wherein the loading a scan test pattern into the scan chain circuit includes loading zero and ones.

20. (original) The method of claim 19, wherein the loading a scan test pattern into the scan chain circuit includes loading an algorithmic scan test pattern.

21. (currently amended) A computer program product containing programming instructions for identifying one or more defective shift register latches in a scan chain,

wherein each of the shift register latches includes a first latch and a second latch connected in a master-slave configuration, wherein each of the first latch and second latch includes at least one clock input, the programming instructions comprising:

placing the scan chain circuit into an operating region;

loading a scan test pattern into the scan chain circuit;

placing the scan chain circuit into a failing region;

applying a shift clock pulse to the clock input of the second latch, wherein the shift clock pulse is applied while the scan chain circuit is in the operating region

placing the scan chain circuit into an operating region; ~~and~~

unloading the scan circuit~~.~~; and

identifying at least one defective shift register latch in the scan chain circuit.

22. (original) A computer program product containing programming instructions for identifying one or more defective shift register latches in a scan chain, wherein each of the shift register latches includes a first latch and a second latch connected in a master-slave configuration, wherein each of the first latch and second latch includes at least one clock input, the programming instructions comprising:

placing the scan chain circuit into an operating region;

loading a scan test pattern into the scan chain circuit;

placing the scan chain circuit into a failing region;

applying a scan lock pulse to the clock input of the first latch, wherein the scan clock pulse is applied while the scan chain circuit is in the operating region;

applying a shift clock pulse to the clock input of the second latch, wherein the shift clock pulse is applied while the scan chain circuit is in the operating region;

placing the scan chain circuit into an operating region; ~~and~~

unloading the scan circuit~~.~~; and

identifying at least one defective shift register latch in the scan chain circuit.